AMENDMENTS TO THE CLAIMS:

1-8. (Canceled)

9. (Previously Presented) A method of fabricating a multilayer semiconductor device, comprising:

forming an metal-insulator-metal (MIM) capacitor including a first metal plate, a dielectric layer formed on the first metal plate, and a second metal plate formed on the dielectric layer;

patterning the second metal plate;

depositing a nitride etch stop layer above the MIM capacitor;

forming an interlayer dielectric on the nitride etch stop layer;

forming a first via and a second via through at least the interlayer dielectric by an anisotropic etch process to contact the nitride etch stop layer above the patterned second metal plate and above the first metal plate, respectively; and

removing portions of the nitride etch stop layer, where the first via and the second via contact the nitride etch stop layer.

10. (Previously Presented) The method of claim 9, wherein patterning the second metal plate comprises patterning by an anisotropic etch process.

11. (Previously Presented) The method of claim 9, wherein removing portions of the nitride etch stop layer comprises removing the portions by a selective via etch chemistry that includes any of the group of argon, nitrogen, C_4F_8 and argon or oxygen, and carbon monoxide.

12. (Previously Presented) The method of claim 9, wherein the depositing of the nitride etch stop layer is directly upon the MIM capacitor.

13. (Previously Presented) The method of claim 9, further comprising patterning at least one of the first metal plate and the dielectric layer by an anisotropic etch process.

14. (Previously Presented) The method of claim 13, further comprising patterning a wiring level in electrical contact with at least one of the first metal plate and the second metal plate by an anisotropic etch process.

15. (Previously Presented) The method of claim 9, further comprising forming a second interlayer dielectric between the second metal plate and the nitride etch stop layer.

16-20. (Canceled)

21. (Previously Presented) The method of claim 9, wherein the depositing includes depositing the nitride etch stop layer on at least the first metal plate and the patterned second metal plate.

22. (Previously Presented) The method of claim 9, wherein removing portions of the nitride etch stop layer comprises removing the portions by a wet etch chemistry.

23. (Previously Presented) A method of fabricating a multilayer semiconductor device including a metal-insulator-metal capacitor (MIM), comprising:

forming a first via and a second via through at least an interlayer dielectric by an anisotropic etch process to contact a nitride etch stop layer above a patterned second metal plate and above the first metal plate of the MIM capacitor, respectively; and

removing portions of the nitride etch stop layer, where the first via and the second via contact the nitride etch stop layer.